1. A group of \_\_\_\_\_\_\_\_\_ connected together forms a register. [ a]

a) Flip-flop b) Counter c) Register d) Latch

2. TTL is a \_\_\_\_\_\_\_\_-circuit and CMOS is a \_\_\_\_\_\_\_\_\_\_circuit. [ a]

a) Driver, load b) Load, Driver c) Both a and b d) None

3. According to manufacturing process involved integrated circuits may be classified as [ c]

a) Monolithic b) Hybrid c) Both a and b d) None

4. A \_\_\_\_\_\_\_\_ is a multi-input, multi-output logic circuit which converts coded inputs into coded outputs

where input and output codes are different. [b ]

a) Encoder b) Decoder c) Multiplexer d) De-multiplexer

5. The propagation delay time of a TTL gate is approximately \_\_\_\_\_\_\_\_\_\_ nano-seconds [d ]

a) 5 b) 8 c) 9 d) 10

6. The IC no. of 8-bit comparator is\_\_\_\_\_\_\_\_ [d ]

a) 7485 b) 74138 c) 74150 d) 74682

7. A 24-bit group ripple adder can be designed using\_\_\_\_\_\_\_\_74283 ICs [c ]

a) 2 b) 4 c) 6 d) 8

8. For divide-by -2 operation, the Flip-Flop must be in the \_\_\_\_\_\_\_\_\_ condition [b ]

a) J=1, K=0 b) J=1, K=1 c) J=0, K=0 d) J=0, K=1

9. Which of the following is not a TTL circuit [c ]

a) 74F00 b) 74AS00 c) 74HC00 d) 74ALS00

10. The noise margin of standard TTL logic is equal to [ b]

a) 0.2 b) 0.4 c) 0.6 d) 0.8

11. The minimum input voltage recognized as HIGH by a TTL gate is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ [a ]

A. 2.0 V B. 2.4 V C. 0.8 V D. 5.0 V

12. Which of the logic families listed below allows the highest operating frequency [ b]

A. 74AS B. ECL C. HCMOS D. 54S

13. A circuit that responds to a specific set of signals to produce a related digital signal

output is called an: [c ]

A. BCD matrix B. Display driver C. Encoder D. Decoder

14. Asynchronous counters are known as [ a]

A. Ripple counters B. Multiple clock counters C. Decade counters D. Modulus counters

15. A 64-bit word consists of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. [b ]

A. 4 bytes B. 8 bytes C. 10 bytes D. 12 bytes

16.In VHDL library clause, the beginning of design file is with [ c ]

(a)Library isse; (b)Library use; (c)Library ieee; (d)Library std\_logic;

17.Simple assigned program of synthesized data flow model [d ]

(a)Y>=A+B (b)Y/=A+B (c)Y\=A+B (d)Y<=A+B

18.Assign operator is used as [b]

(a)< (b)<= (c)>= (d)/=

19.\_\_\_\_\_\_\_\_\_\_\_\_\_ is a 4 bit binary adder [ a ]

(a)74x283 (b)74x280 (c)74x138 (d)74x153

20.’If then else’ VHDL statement is used within [ a ]

(a)process (b)While (c) Select (d)Assert